Claims:

What is claimed is:

1. A method of stabilizing chrominance subcarrier generation in a video signal comprising the steps:

   a. calculating a time shift occurring in an output waveform;

   b. converting the time shift into an equivalent phase shift; and

   c. sending a phase correction number to a waveform generator block according to the equivalent phase shift.

2. The method according to claim 1 wherein the time shift is calculated for each video line.

3. The method according to claim 1 wherein calculating a time shift in an output waveform comprises:

   a. calculating DELT, the amount of time the output waveform is shifted; and

   b. calculating TAV, the average period of the output waveform.

4. The method according to claim 3 wherein the amount of time the output waveform is shifted DELT is given by:

$$DELT = B*TAU$$

where B is the sum of a sequence of digital numbers outputted by a limiter and TAU is a delay of one delay element.

5. The method according to claim 3 wherein the average period of the output waveform

TAV is given by:

$$TAV = (2^m/F2)*((32-Q)*TAU)$$

where TAU is the delay of one delay element, F2 is the frequency control number from a subcarrier phase locked loop, Q is an average value of a clockout period and m is a number of bits stored in a register.

6. The method according to claim 1 wherein converting the time shift to an equivalent phase shift of the output waveform DELP is given by:

$$DELP = Fracof*((B*F2)/(2^m*(32-Q)))*360$$

where B is the sum of a sequence of digital numbers outputted by a limiter, F2 is the frequency control number from a subcarrier phase locked loop, Q is an average value of a clockout period, m is a number of bits stored in a register and Fracof is a fractional cycle shift.

7. The method according to claim 1 wherein sending a phase correction number PHQ to a waveform generator block according to the equivalent phase shift is given by:

$$PHQ = Fracof*((-B*F2)/(2^m*(32-Q)))*2^k$$

where k is the number of bits in a look up table, B is the sum of a sequence of digital numbers outputted by the limiter, F2 is the frequency control number from a subcarrier phase locked loop, Q is the average value of a clockout period, m is the number of bits stored in a register and Fracof is the fractional cycle shift.

8. The method according to claim 1 wherein the phase correction number will remove the phase shift from the output waveform.

9. The method according to claim 1 wherein the phase correction number will be sent to a waveform generator block according to the equivalent phase shift for each video line.

10. An apparatus for stabilizing chrominance subcarrier generation in a video signal, the apparatus comprising:

a. a clock generator circuit;

b. a digital phase detector;

c. a digital loop filter;

d. a waveform generator; and

e. a phase correction block.

11. The apparatus of Claim 10 wherein the apparatus may also comprise a serializer.

12. The apparatus of Claim 10 wherein the clock generator circuit includes:

a. an oscillator;

b. a phase accumulator/logic block;

c. a multiplexor;

d. a phase comparator; and

e. a plurality of delay elements.

13. The clock generator circuit of Claim 12 wherein the plurality of delay elements are coupled serially in a ring formation such that an output of the last delay element is coupled to the input of the first delay element.

14. The clock generator circuit of Claim 12 wherein each of the plurality of delay elements have an identical delay time.

15. The clock generator circuit of Claim 12 wherein the oscillator generates a CLOCKIN signal.

16. The clock generator circuit of Claim 12 wherein the CLOCKIN signal is coupled with a first input of the phase comparator.

17. The clock generator circuit of Claim 12 wherein the output of the plurality of delay elements is also coupled to a second input of the phase comparator.

18. The clock generator circuit of Claim 12 wherein an output of the phase comparator is coupled with each of the plurality of delay elements in order to effectuate delay adjustment.

19. The clock generator circuit of Claim 12 wherein an output of each of the plurality of delay elements is coupled with a corresponding input of the multiplexor.

20. The clock generator circuit of Claim 12 wherein the CLOCKIN signal and the output of the last delay element are compared in the phase comparator.

21. The clock generator circuit of Claim 12 wherein the phase comparator adjusts the delay of each of the plurality of delay elements such that a combined delay of the plurality of delay

elements is equal to one cycle of the CLOCKIN signal.

22. The apparatus of Claim 10 wherein the digital loop filter consists of a K1 path and a K2 path.

23. The digital loop filter of Claim 22 wherein a phase error for each video line coming from the digital phase detector is inputted into the K2 path that includes:

a. a first scaler;

b. a first summer;

c. a first limiter;

d. a first register; and

e. an accumulator block.

24. The K2 path of Claim 23 wherein the first scaler multiplies the phase error by a constant K2.

25. The K2 path of Claim 23 wherein the first summer sums an output of the first scaler with an output Q of the first register..

26. The K2 path of Claim 23 wherein an output of the first summer is coupled with an input of the first limiter.

27. The K2 path of Claim 23 wherein an output of the first limiter is coupled with an input of the first register.

28. The K2 path of Claim 23 wherein the output Q of the first register is coupled with an input of the first summer.

29. The K2 path of Claim 23 wherein the K2 path is split into an upper K2 path and a lower K2 path.

30. The K2 path of Claim 23 wherein the lower bits from the output Q are coupled with the accumulator block of the lower K2 path.

31. The K2 path of Claim 23 wherein the upper bits from the output Q are coupled with the upper K2 path.

32. The digital loop filter of Claim 23 wherein the phase error for each video line coming from the digital phase detector is inputted into the K1 path that includes:

a. a second scaler;

b. a second limiter;

c. a second register;

d. a second summer; and

e. a third limiter.

33. The K1 path of Claim 32 wherein the second scaler multiplies the phase error by a constant K1.

34. The K1 path of Claim 32 wherein an output of the second scaler is coupled with an input of the second limiter.

35. The K1 path of Claim 32 wherein an output B of the second limiter is coupled with a first input of the second register.

36. The K1 path of Claim 32 wherein an output of the second register is coupled with an input of a third limiter.

37. The K1 path of Claim 32 wherein the output of the second register is coupled with an input of a second summer.

38. The K1 path of Claim 32 wherein the ~~an~~ output +/- L of the third limiter is coupled with the input of the second summer.

39. The K1 path of Claim 32 wherein a sum of the second summer is coupled with a second input of the second register.

40. The digital loop filter of Claim 22 wherein the output +/- L of the third limiter, the upper bits in the K2 path and an output OB of the accumulator block of the lower K2 path are coupled with an input of a third summer.

41. The digital loop filter of Claim 22 wherein an output of the third summer is coupled with an input of a fourth limiter.

42. The digital loop filter of Claim 22 wherein an output of the fourth limiter is coupled with an input of the phase accumulator logic block in the clock generator circuit.

43. The clock generator circuit of Claim 12 wherein at least one output of the phase accumulator logic block is coupled with a corresponding input of the multiplexor.

44. The digital loop filter of Claim 22 wherein the output B of the second limiter and the output Q of the first register are coupled with an input of the phase correction block.

45. The apparatus of Claim 10 wherein an output PHQ of the phase correction block is coupled to either the serializer or the waveform generator.

46. The apparatus of Claim 10 wherein an output of the serializer is coupled with the waveform generator.